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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H03M 1/10, 1/14

A1

(11) International Publication Number: WO 95/20270

(43) International Publication Date: 27 July 1995 (27.07.95)

(21) International Application Number: PCT/US94/10318

(22) International Filing Date: 12 September 1994 (12.09.94)

(30) Priority Data:
08/183,679 19 January 1994 (19.01.94) US

(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; 1090 Kifer Road, M/S 16-135, Sunnyvale, CA 95086-3737 (US).

(72) Inventors: MAYES, Michael, K.; 1326 Shelby Creek Lane, San Jose, CA 95120 (US). CHIN, Sing, W.; 21 Beaufort Harbor, Alameda, CA 94501 (US).

(74) Agent: RODDY, Richard, J.; National Semiconductor Corporation, 1090 Kifer Road, M/S 16-135, Sunnyvale, CA 94086-3737 (US).

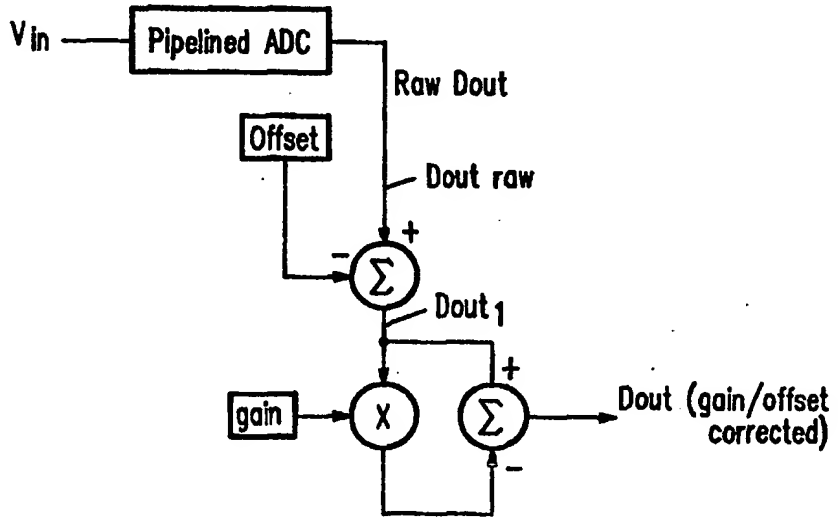
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: PIPELINED ANALOG-TO-DIGITAL CONVERTER WITH CURVEFIT DIGITAL CORRECTION

(57) Abstract

An ADC system in which raw ADC data is received and digitally manipulated to increase the accuracy of the resultant digital output word. In one embodiment, the digital manipulation of this invention is performed on data which has been preliminarily adjusted for errors caused by use of an interstage gain less than ideal. In one embodiment, digital correction is performed based only on the errors of a plurality of most significant bit stages, rather than all stages, as the effect on error of the digital output word is of decreasing importance for stages of less significance. In accordance with one embodiment of this invention, offset error and full scale error are determined by applying ±Vref as an input signal to the ADC. These values allow the raw digital data from the ADC to be compensated in either hardware or software to provide a more accurate digital representation of the analog input voltage being measured. In accordance with another embodiment of this invention, second order errors are removed by determining the magnitude of, par example, capacitor value voltage coefficients of the MSB stage of the ADC after calibration of lesser significant bit stages, and using these voltage coefficients to further adjust the digital output word, providing an even more accurate digital representation of the analog input signal being mesured.



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PIPELINED ANALOG-TO-DIGITAL CONVERTER WITH CURVEFIT DIGITAL CORRECTION

Background of the Invention

This invention pertains to analog-to-digital converters, and more specifically to pipelined analog-to-digital converters which, in accordance with the teachings of this invention, utilize digital correction features.

Description of Prior Art

The typical N-bit pipelined analog-to-digital converter (ADC) consists of N 1-bit stages which, as shown in Figure 1, each include a comparator 11, summing element 12, and gain element 13.

The analog input signal Vin to stage 10 is multiplied by 2 by gain element 13. A reference voltage Vref is either added to or subtracted from 2*Vin by summing element 12, depending upon the digital input signal Din to stage 10. The resultant residual voltage

$$Vres = 2Vin \pm Vref \qquad (1)$$

is applied the next stage. The polarity of residual voltage Vres is detected by comparator 11, whose output signal Dout serves as the digital input signal Din of the next stage. Cascading N similar stages 10-1 through 10-N results in an N-bit Analog-to-Digital converter, as shown in Figure 2, where the residual voltages of each stage are defined by equations (2), (3) and (4). Also shown in Figure 2 is a "zeroth" stage 10-0, providing an N+1 bit ADC, which is the sign of the input voltage Vin. In the example of Figure 2, stage 10-0 includes a one-times multiplier (for example, just a wired connection), and a comparator. The residual voltages for subsequent stages are based on the preceding stages:

$$Vres_1 = 2\left(Vin \pm \frac{Vref}{2}\right) \qquad (2)$$

$$Vres_2 = 2\left(Vres_1 \pm \frac{Vref}{2}\right) \qquad (3)$$

$$Vres_N = 2\left(Vres_{N-1} \pm \frac{Vref}{2}\right) \qquad (4)$$

Ideally, the transfer function of each stage is given by Equation 1 (for an input voltage of Vin), and is shown in graphical form in Figure 3, having two segments defined by equations (5) and (6).

$$Vres = 2\left(Vin + \frac{Vref}{2}\right) \qquad (5)$$

$$Vres = 2(Vin - \frac{Vref}{2}) \quad (6)$$

However, capacitor mismatch errors, charge injection, operational amplifier offset voltages, parasitic capacitance, and finite operational amplifier gain result in variations in the single stage transfer function, as graphically depicted in Figures 4a-4d with a solid line, as differentiated from the ideal transfer function shown as the shaded line. Figure 4a shows the ideal transfer function and the actual transfer function for a stage in which the gain factor of gain element 13 (Figure 1) is less than 2 as caused, for example, by capacitor mismatch; Figure 4b shows the ideal and actual transfer functions for a stage in which the gain is greater than 2 as caused, for example, by capacitor mismatch; Figure 4c shows the ideal and actual transfer function for a stage in which reference mismatch errors cause vertical shift; and Figure 4d shows the ideal and actual transfer functions of a stage in which charge injection in the comparator feedback switch causes a comparator offset. Naturally, various ones of these transfer function errors are combined in an actual device.

The gain error of a pipelined stage is due to capacitor mismatches (typically 0.10% for double-layer polycrystalline silicon capacitors). As the ratio varies due to capacitor mismatch, the gain varies, as shown in Figures 4a and 4b. Gain element 13 includes an operational amplifier which inherently has finite gain and offset errors.

The residual voltage (Vres) is the combination of 2*Vin and ±Vref. Variations in the capacitor matching lead to a vertical shift in the transfer function, as shown in Figure 4c.

$$Vres = 2Vin \pm Vref + \alpha \quad (7)$$

where α is a constant error in reference voltage Vref.

Ideally, the digital input signal Din is given by

$$Din = 0, for\ Vin < 0 \quad (8)$$

$$Din = 1,\ Vin > 0 \quad (9)$$

However, charge injection in comparator 11 causes a variation in the comparison point, resulting in a horizontal shift in the transfer function, as shown in Figure 4d.

The combination of all these error mechanisms applied to a pipelined ADC limits the resolution of the ADC. Furthermore, redundancy must be added to the converter to account for overrange errors in which the transfer function exceeds ±Vref (see Figures 4b and 4c). This is done by using a gain less than 2 for each stage. Therefore, a 16-bit Pipelined ADC with 0.1% capacitor matching, 10mV of charge injection, 10mV of operational amplifier offset, a finite operational amplifier gain of 10,000, and an intra-stage gain of 1.97 results in a 1200 LSB linearity error, as depicted in Figure 5. Figure 5 is a graph having ADC code values (i.e., digital output words) on its X-axis, and the error, as measured in a multiple of the least significant bit

value, displayed on its Y-axis. As shown in Figure 5, for the criteria established for this example, a maximum error of approximately 1200 LSB is the undesirable result.

Charge injection, gain, and reference errors can be removed by using known techniques, such as self-calibration techniques, trimming capacitor values and reference values, and the use of dummy devices to minimize charge injection.

The majority of linearity errors is due to the use of a 1.97 gain factor rather than the ideal gain factor of 2. It is known to remove these errors by calculating three coefficients per stage, K_0, K_1, and K_2 (see Figure 6), and applying them to the raw output data. Once these coefficients K_0, K_1 and K_2 are known for each stage, the linearity error can be corrected, as described in _1993 IEEE International Solid-State Circuits Conference, Session 4, Paper WP 4.2. Figure 7 shows the progression of linearity correction starting with calibrating LSB stage 10-N (i.e. stage 10-16 for an ADC where N=16), and progressing towards the calibration of successively more significant bit stages to the most significant bit stage 10-1. The resulting linearity has a large fullscale and offset error.

Thus, even by utilizing known techniques for minimizing the effects of charge injection, gain errors, and reference voltage errors, as well as the more complex prior art technique of calculating three digital coefficients per stage for application to the raw, uncalibrated output data as correction factors, a significant error remains in analog-to-digital converters. Accordingly, there remains the need to provide further accuracy in analog-to-digital conversions.

Summary

A novel analog to digital converter system is taught in which raw ADC data is received and digitally manipulated in one or more ways in order to increase the accuracy of the resultant digital output word representing the analog input voltage being measured. In one embodiment, the digital manipulation of this invention is performed on data which has been preliminarily adjusted for errors caused by use of an interstage gain less than ideal.

In one embodiment, digital correction is performed based only on the errors of a plurality of most significant bit stages, rather than all stages, as the effect on error of the digital output word is of decreasing importance for stages of less significance.

In accordance with one embodiment of this invention, offset error and full scale error are determined by applying ±Vref as an input signal to the ADC. These values allow the raw digital data from the ADC to be compensated in either hardware or software to provide a more accurate digital representation of the analog input voltage being measured.

In accordance with another embodiment of this invention, second order errors are removed by determining the magnitude of, for example, the error due to capacitor voltage coefficients of the MSB stage of the ADC after calibration of lesser significant bit stages, and using these voltage coefficients to further adjust the digital output word, providing an even more accurate digital representation of the analog input signal being measured.

Brief Description of the Drawings

Figure 1 is a diagram depicting a typical prior art 1-bit analog to digital converter stage;

Figure 2 is a diagram of a typical prior art N+1 bit analog to digital converter;

Figure 3 is a graph of the transfer function of an ideal analog to digital converter stage of Figure 1;

Figures 4a-4d are graphs depicting nonideal transfer functions due to various inaccuracies in implementing the analog to digital converter stage of Figure 1;

Figure 5 is a graph depicting ADC code values verses error for a typical prior art analog to digital converter;

Figure 6 is a graph of a transfer function for selected input voltages applied to an analog to digital converter to establish coefficients K_0, K_1, and K_2, in accordance with a prior art error correction technique;

Figure 7 is a set of graphs depicting improving linearity with increasing number of stages calibrated;

Figure 8a depicts a transfer function of an analog to digital converter stage having gain error and residual voltage error;

Figure 8b depicts a transfer function of an analog to digital converter stage showing linerarity error;

Figure 9 is a block diagram depicting an analog to digital converter and circuitry for applying ±Vref to its input for calibration in accordance with this invention;

Figure 10a is a graph depicting linearity error after calibrating out single stage gain and charge injection errors;

Figure 10b is a block diagram depicting an analog to digital converter together with digital correction stages, in accordance with this invention;

Figure 11 is a graph depicting the resulting linearity error for an exemplary analog to digital converter including digital correction in accordance with this invention;

Figure 12 is a block diagram depicting calibration of a first MSB stage, once subsequent LSB stages have been calibrated;

Figure 13 is a block diagram depicting an analog to digital converter including digital correction features as taught by the present invention; and

Figure 14 is a graph depicting the improvement in analog to digital converter accuracy as a result of the second order calibration feature of the present invention.

Detailed Description

One important characteristic of a pipelined ADC is the attenuation of error with respect to stage number. For example, the first (i.e. most significant bit) stage contributes 100% of its mismatches to the final linearity. However, the second stage is isolated from the input by a gain of 2, leading to a 50% contribution to the overall system errors. Similarly, the third stage errors are reduced to 25% and the forth to 12.5% and so on. Based on this feature of pipelined ADCs, in accordance with this exemplary embodiment of the present invention, curvefit calibration is only applied to the first four stages (i.e. the most significant stages 10-1 through 10-4 of the exemplary ADC circuit of Figure 2), which results in an error of less than 1 LSB. Naturally, it will be appreciated by those of ordinary skill in the art in light of the teachings of this invention that the curvefit calibration taught by this invention can be applied to any number of stages in a pipelined ADC, depending on the desired amount of accuracy.

A second characteristic of a pipelined ADC is the inherent analog "multimeter" contained within the pipe. For the moment, consider a 16-bit ADC (having stages 10-0 through 10-16), in which stage 10-1 is non-ideal with a constant gain error and an associated residual voltage error as shown in Figure 8a, while all remaining stages (stages 10-2 through 10-16) are ideal. A linearity sweep of an ADC under these conditions, as shown in Figure 12, results in linearity errors whose signature matches the signature of the non-ideal stage 10-1, as depicted in the graph of Figure 8b. This inherent feature of pipelined ADCs allows calibration of a given stage once stages for less significant bits have been calibrated.

Calibration of stages 10-6 through 10-16 using prior techniques, such as explained above, leads to large gain and offset errors. For interstage gain of 1.97, the gain error is in excess of 20,000 LSB (see Figure 7). By way of example, the integral non-linearity is calculated using a 16-bit pipelined ADC with 10ppm/volt second order capacitor voltage coefficient. As is known, by using a differential signal path, first order capacitor voltage coefficient is cancelled. Figure 10a shows the linearity error after calibrating out the single-stage gain and charge injection errors. This is the resulting linearity of prior art ADC circuits after the calculation of K_0, K_1 and K_2 for stages 10-6 through 10-16 prior to the curve-fit calibration of the present invention.

Applying +Vref and -Vref as the input signal Vin to the pipelined ADC as shown in Figure 9, the ADC offset and ADC gain errors are determined. Digital correction terms are generated by applying +Vref to the ADC to measure the ADC fullscale error and by applying -Vref to measure the ADC offset error. The first correction term, gain, given by

$$gain = \frac{fullscale\ error - offset\ error}{2^N} \qquad (10)$$

allows adjustment of the slope of the linearity, for example by using a multiplier. Note that the denominator in equation (10) is equal to 65536 (2^{16}), the number of possible output codes from the ADC when the ADC contains 16 stages, by way of example. The second correction term, offset, allows for adjustment of the offset of the linearity, for example by using an adder. For each normal conversion cycle, the raw digital output Dout(raw) is modified using gain and offset correction factors, as shown by Equations 11 and 12.

$$Dout_1 = Dout(raw) - offset \qquad (11)$$

and, following this step,

$$Dout(g/o\ corrected) = Dout_1 - Dout_1 \times gain \qquad (12)$$

where Dout(g/o corrected) is a digital output word including correction for gain and offset errors.

Once the offset and gain are calibrated, the linearity error is, for an exemplary 16 bit ADC, on the order of 2LSB (14 bits accurate), as shown in Figure 11. Figure 10b is a block diagram of a structure in accordance with the teachings of this invention suitable for implementing the correction factors exemplified by equations (11) and (12).

Figure 9 depicts how MSB stage 10-1 is calibrated in accordance with the teachings of this invention for removing the "system gain" and "system offset" errors.

Measurement of Second Order Coefficient

Assuming stages 10-2 through 10-N were previously calibrated, for example by using techniques known in the prior art as well as the offset and gain calibration of this invention as described above, they may be used to measure the linearity of the first stage, stage 10-1 and the ADC gain error and ADC offset error. A capacitor voltage coefficient error on the first stage results in a hyperbolic type transfer function in the linearity plot. This hyperbola has its vertices at ±Vref/2, which, for a typical ADC operating with a Vcc of 5 volts, and thus using a Vref of 5 volts, this hyperbola has its vertices at approximately plus and minus 2.5 volts, as shown in Figure 11.

Ideally, (no voltage coefficient) the digital output words are equal to:

$$Dout = 16384 \text{ for } Vin = -2.5v \quad (13)$$

$$Dout = 49152 \text{ for } Vin = +2.5v \quad (14)$$

However, when an inherent and undesirable error of, for example, a 10ppm of capacitors second order voltage coefficient in the first stage 10-1, Dout is changed:

$$Dout = 16384 + E_1 \text{ for } Vin = \frac{-Vref}{2} \quad (15)$$

$$Dout = 49152 - E_2 \text{ for } Vin = \frac{+Vref}{2} \quad (16)$$

where E_1 and E_2 are digital values representing the error introduced by the 10ppm voltage coefficient in the first stage for Vin = -Vref/2 and Vin = +Vref/2, respectively.

By applying exactly ±Vref/2 to the input of the first stage 10-1 after calibration of stages 10-2 through 10-N (see Figure 12), the values of E_1 and E_2 are determined. As an example, for a capacitor voltage coefficient of 10ppm, this results in

$$E_1 = 2.1 \, LSB \quad (17)$$

$$E_2 = 2.1 \, LSB \quad (18)$$

Once E_1 and E_2 have been determined, generated coefficients allow the adjustment of the gain/offset corrected digital output word to provide the final digital output word Dout(final), as depicted in Figure 13.

The second order correction coefficients are defined as:

$$SEC_1 = \frac{E_1}{(output:-Vref/2)^2} \quad (19)$$

$$SEC_2 = \frac{E_2}{(output:+Vref/2-sign\ bit)^2} \quad (20)$$

where output:-Vref/2 is equal to the digital output word for an ideal situation (i.e. without any error) when the ADC receives an input voltage of -Vref/2. In the example where N=16 and Vref=5 volts, this value output:-Vref/2 is equal to 16384. Similarly, output:+Vref/2-sign bit is equal to the digital output word for an ideal situation when the ADC receives an input voltage of +Vref/2, minus the digital value of the sign bit. In the example in which N=16 and Vref=5 volts, output:+Vref/2 is equal to 49152 and the digital value of the sign bit is equal to 32768, and thus the value of output:+Vref/2 - sign bit is equal to 16384.

This results in the following operations on the gain/offset corrected version of Dout (Dout(g/o corrected) from the operation of equations (11) and (12), for example by the exemplary circuitry of Figure 10b) to provide a final value Dout(final):

$$\begin{array}{c} if\ sign\ bit=1, then \\ Dout(final) = \\ Dout(g/o\ corrected) + (SEC_2)\ (Dout(g/o\ corrected) - 49152)^2 \end{array} \quad (21)$$

$$\begin{array}{c} if\ sign\ bit=0, then \\ Dout(final) = \\ Dout(g/o\ corrected) + (SEC_1)\ (Dout(g/o\ corrected) - 16384)^2 \end{array} \quad (22)$$

Figure 14 is a graph depicting a first curve Dout(g/o correction) showing a rather significant second order voltage coefficient existing after gain and offset calibration as taught by the present invention, but prior to second order calibration. The second curve Dout(final) of Figure 14 shows the much improved second order voltage coefficient resulting from second order calibration in accordance with the teachings of this invention. Second order calibration, with linear gain and offset calibration, improves the total unadjusted error to 1/4 LSB accuracy with no offset or fullscale error.

Thus in accordance with the teachings of this invention several digital correction techniques are taught for improving the accuracy of pipelined analog to digital converters, by determining the nature of the inherent inaccuracies of the analog to digital converter and manipulating the raw digital result from the ADC to provide a digitally corrected highly accurate output word. While the examples given above show digital correction being performed using dedicated digital adders and multipliers, it will be appreciated by those of ordinary skill in the art in light of the teachings of this invention that other types of digital manipulation, such as with microprocessors or table look up features, can be used without departing from the spirit of this invention.

All publications and patent applications mentioned in this specification are herein incorporated by reference to the same extent as if each individual publication or patent application was specifically and individually indicated to be incorporated by reference.

The invention now being fully described, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the spirit or scope of the appended claims.

WHAT IS CLAIMED IS

1. An analog to digital converter system comprising:

an analog to digital converter circuit for receiving an analog input signal and providing a raw digital output word representing said analog input signal; and

digital circuitry for receiving said raw digital output word and providing a final digital output word representative of said analog input signal, said digital circuitry modifying said raw digital output word to adjust for errors in the gain and inherent offsets of said analog to digital converter circuit.

2. An analog to digital converter system as in claim 1 which further comprises a circuit to apply a first reference voltage as said analog input signal to obtain a digital output word indicative of said offset errors and a second reference voltage as said analog input signal to obtain a digital output word indicative of said gain errors.

3. An analog to digital converter system as in claim 2 wherein said second reference voltage is the same magnitude and opposite sign as said first reference voltage.

4. An analog to digital converter system as in claim 2 wherein said digital circuitry comprises a summer for adjusting said raw digital output word to correct for said offset errors.

5. An analog to digital converter system as in claim 2 wherein said digital circuitry comprises a multiplier for adjusting said raw digital output word to correct for said gain errors.

6. An analog to digital converter system as in claim 2 wherein said digital circuitry comprises a processor for adjusting said raw digital output word to correct for said offset errors.

7. An analog to digital converter system as in claim 2 wherein said digital circuitry comprises a procesor for adjusting said raw digital output word to correct for said gain errors.

8. An analog to digital converter system as in claim 1 which further comprises circuitry for calibrating one or more LSB stages of said analog to digital converter circuit prior to determining said gain and offset errors.

9. An analog to digital converter system as in claim 2 wherein said analog to digital converter circuit uses reference voltages of ±Vref, and said first and second reference voltages are ±Vref.

10. An analog to digital converter system as in claim 2 which further comprises circuitry for applying third and fourth reference voltages as said analog input signal to obtain digital words indicative of second order errors.

11. An analog to digital converter system as in claim 10 wherein said fourth reference voltage is the same magnitude and opposite sign as said third reference voltage.

12. An analog to digital converter system as in claim 10 wherein said digital circuitry comprises a summer for adjusting said raw digital output word to correct for said second order errors.

13. An analog to digital converter system as in claim 10 wherein said digital circuitry comprises a processor for adjusting said raw digital output word to correct for said second order errors.

14. An analog to digital converter system as in claim 10 wherein said analog to digital converter circuit uses reference voltages of ±Vref, and said third and fourth reference voltages are ±Vref/2.

15. A method for calibrating an analog to digital converter system comprising the steps of:

calibrating a plurality of LSB stages;

applying a first reference signal to said analog to digital converter to obtain a first digital output word indicative of the offset error of one or more uncalibrated MSB stages; and

applying a second reference signal to said analog to digital converter to obtain a second digital output word indicative of the gain error of said one or more uncalibrated MSB stages.

16. A method as in claim 15 wherein said analog to digital converter system used as reference voltages ±Vref, and said first an second reference signals are ±Vref.

17. A method as in claim 15 which further comprises the steps of:

applying third and fourth reference voltages to said analog to digital converter system to determine a second order error coefficient.

18. A method as in claim 17 wherein said third and fourth voltages are equal to ±Vref/2.

19. A method for operating an analog to digital converter system comprising the steps of:

calibrating a plurality of LSB stages;

applying a first reference signal to said analog to digital converter to obtain a first digital output word indicative of the offset error of one or more uncalibrated MSB stages;

applying a second reference signal to said analog to digital converter to obtain a second digital output word indicative of the gain error of said one or more uncalibrated MSB stages; and

applying an unknown analog input signal to said analog to digital converter to obtain a raw digital output word indicative of said analog input signal;

modifying said raw digital output word utilizing said first digital output word in order to provide a final digital output word which more accurately represents said analog input signal.

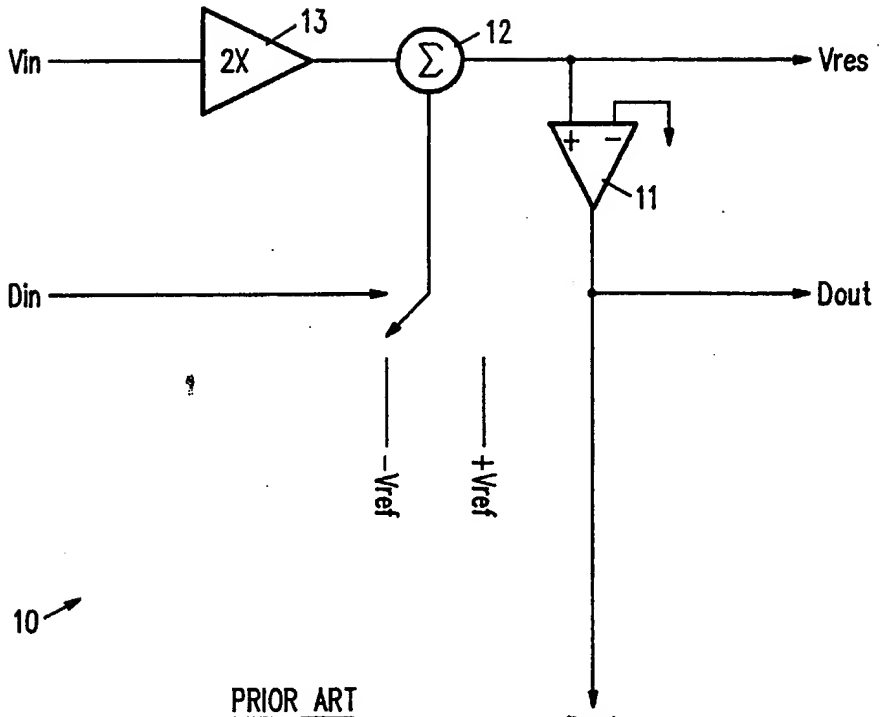
20. A method as in claim 19 wherein said analog to digital converter system used as reference voltages ±Vref, and said first an second reference signals are ±Vref.

21. A method as in claim 19 which further comprises the steps of:

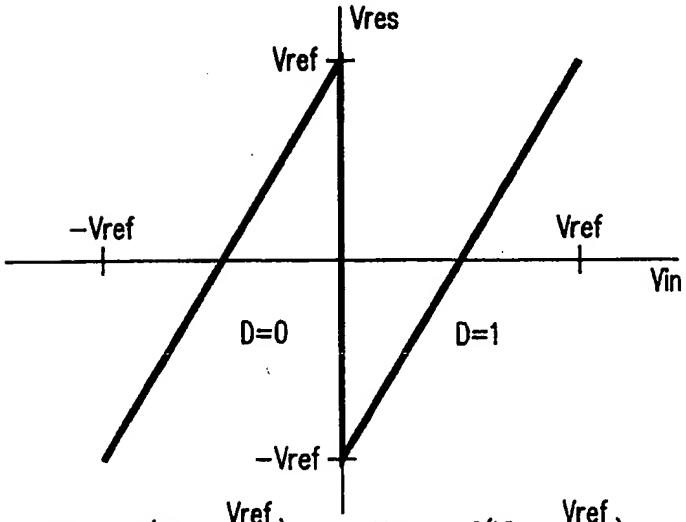
applying third and fourth reference voltages to said analog to digital converter system to determine a second order error coefficient.

22. A method as in claim 21 wherein said third and fourth voltages are equal to ±Vref/2.

23. A method as in claim 17 which further comprises a step of modifying said raw digital output word in response to said second order error coefficient to provide said final digital output word.

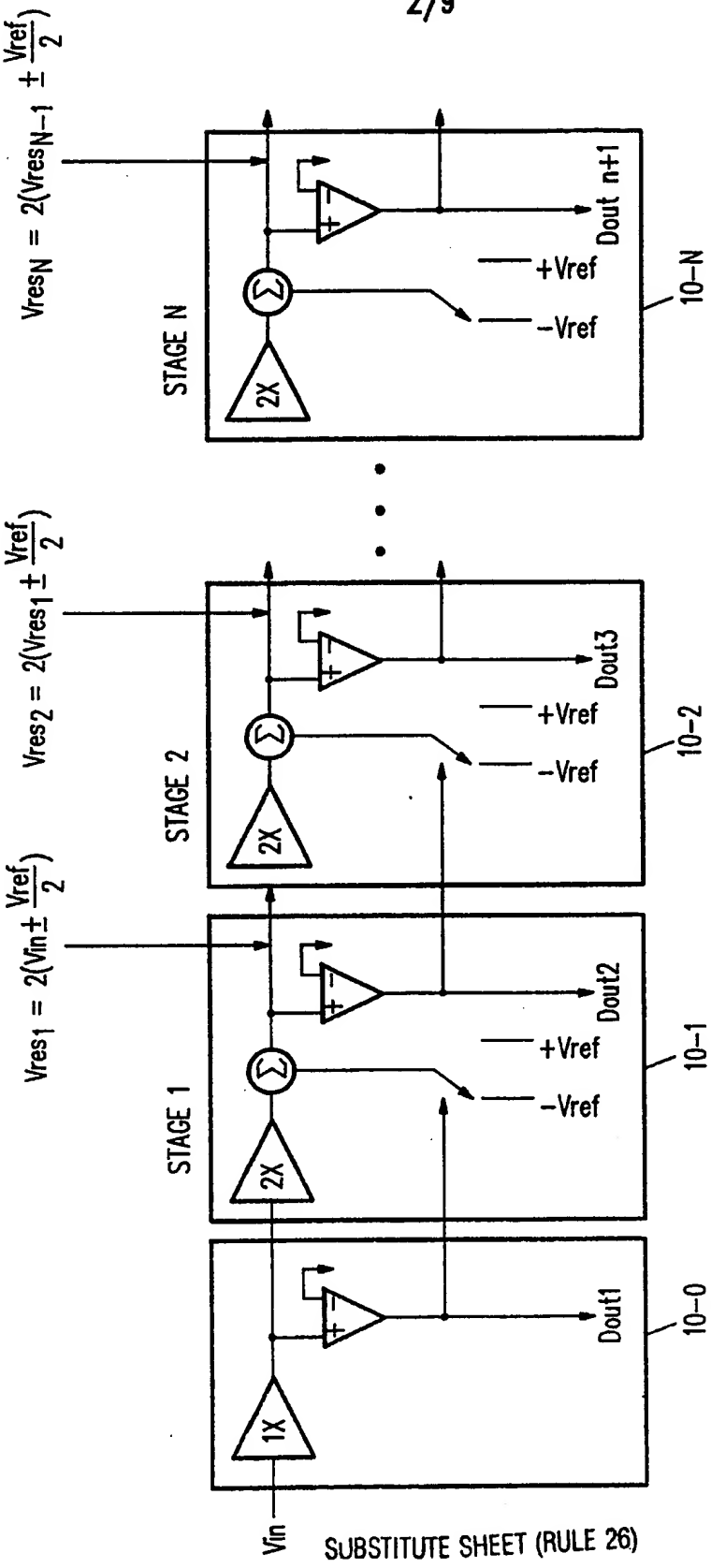


PRIOR ART
FIG. 1

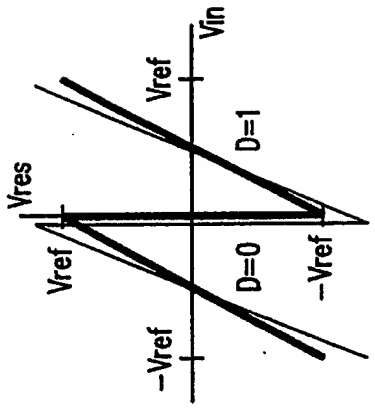


$$Vres = 2(Vin + \frac{Vref}{2}) \qquad Vres = 2(Vin - \frac{Vref}{2})$$

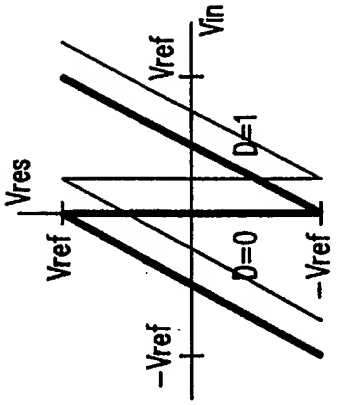
PRIOR ART
FIG. 3



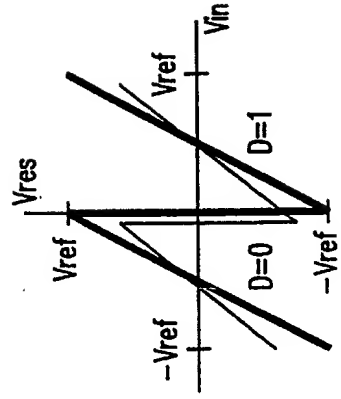
PRIOR ART
FIG. 2



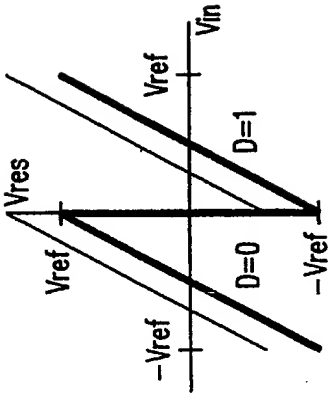
PRIOR ART
FIG. 4b



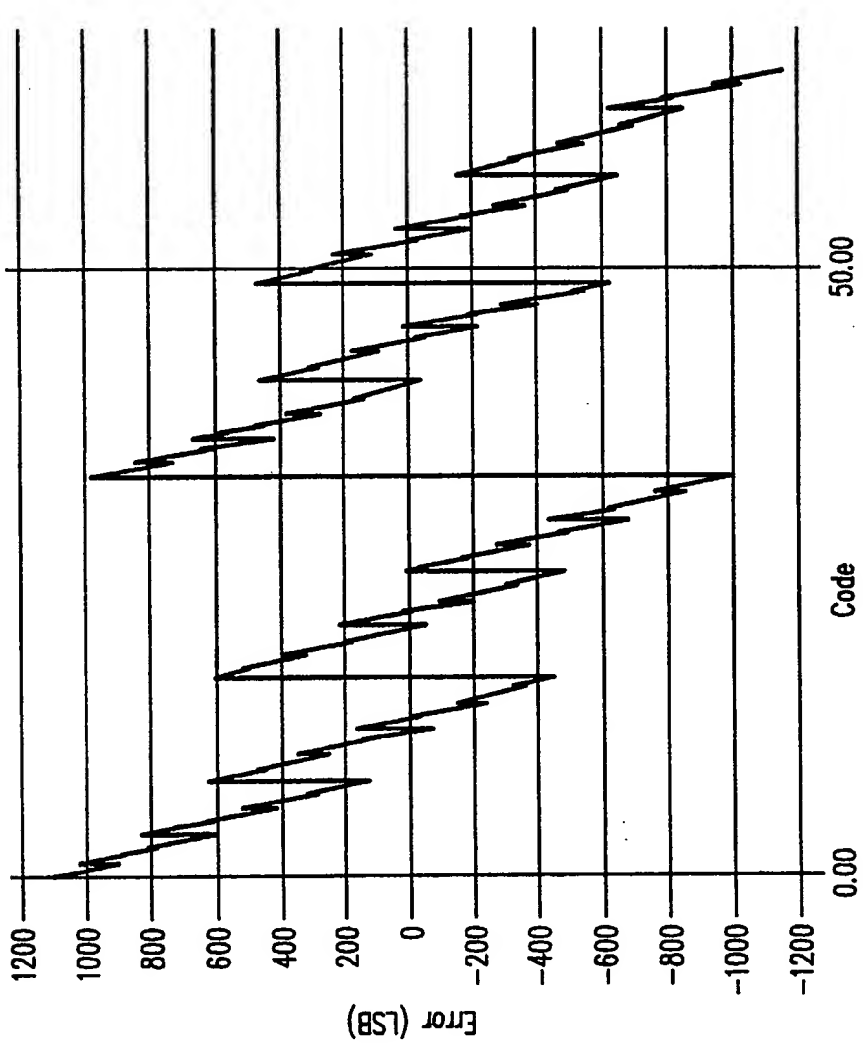
PRIOR ART
FIG. 4d



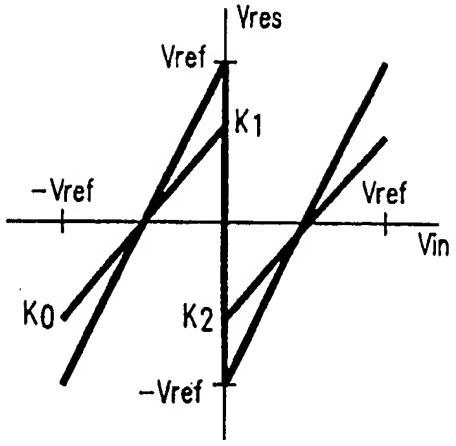
PRIOR ART
FIG. 4a



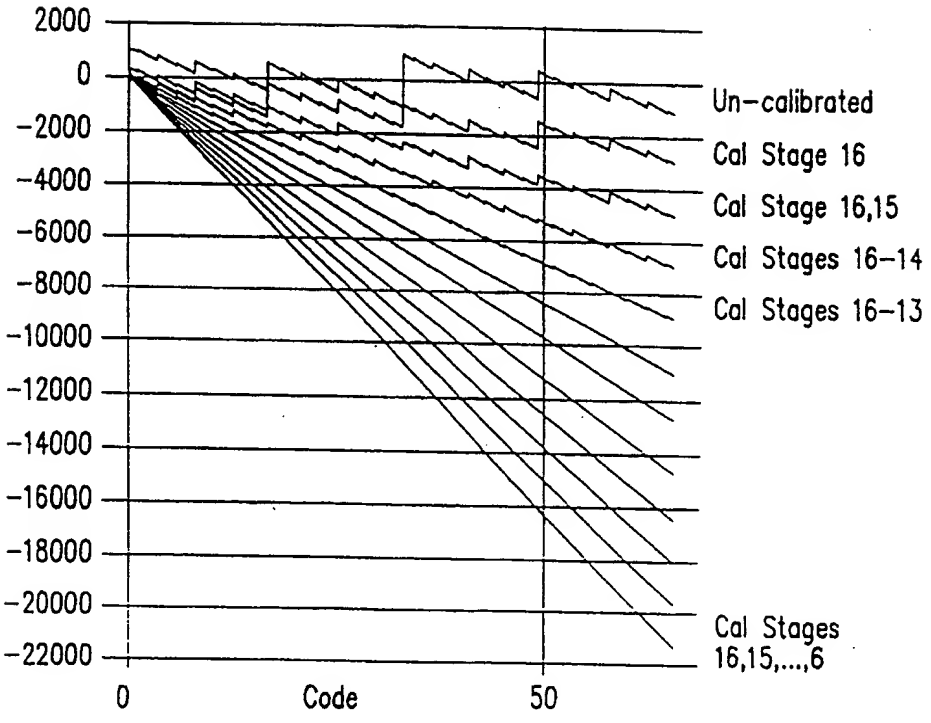
PRIOR ART
FIG. 4c



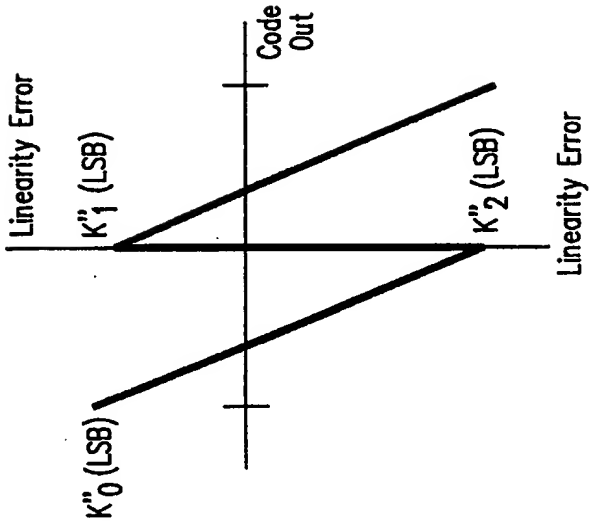
PRIOR ART
FIG. 5



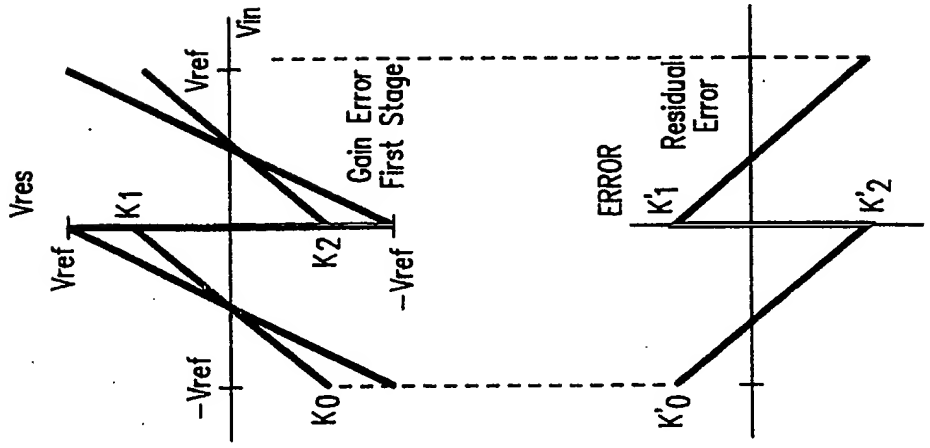
PRIOR ART
FIG. 6



PRIOR ART
FIG. 7



PRIOR ART
FIG. 8b



PRIOR ART
FIG. 8a

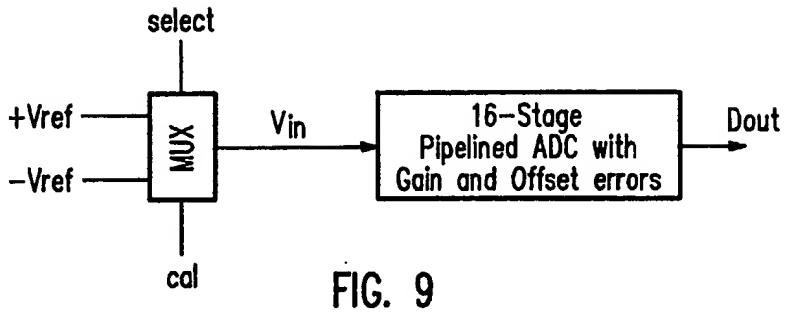


FIG. 9

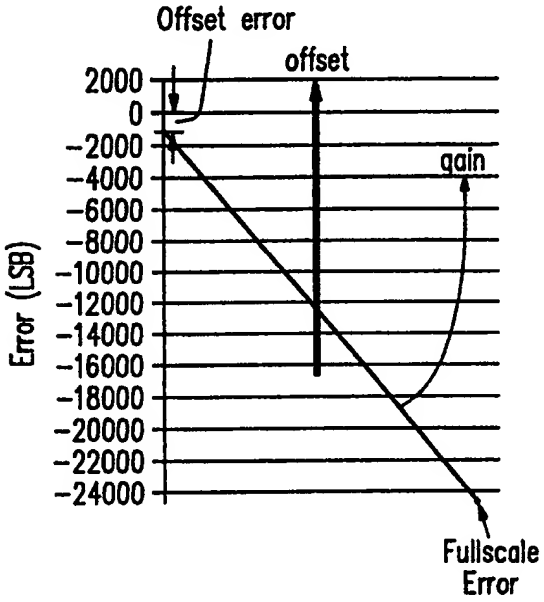


FIG. 10a

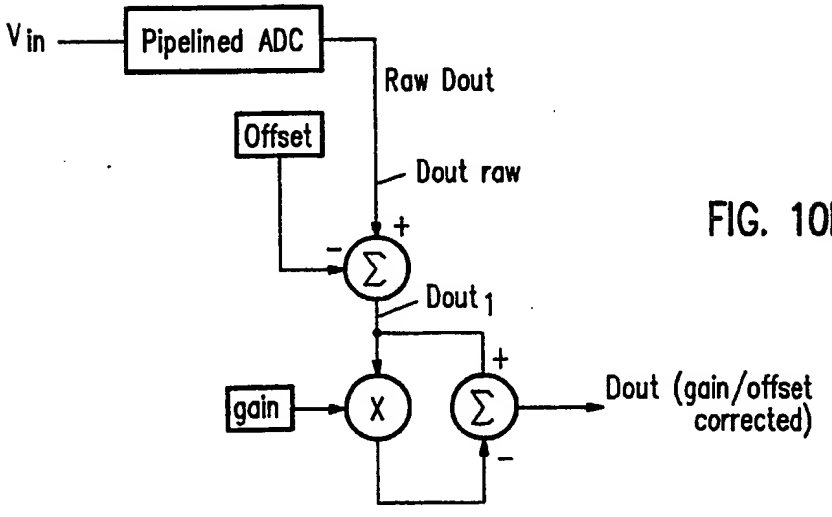


FIG. 10b

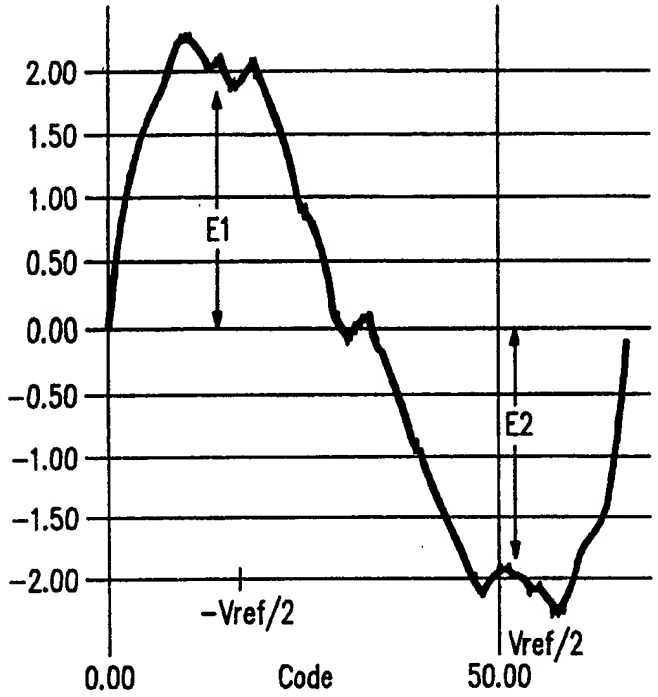

2.00
1.50
1.00
0.50
0.00
-0.50
-1.00
-1.50
-2.00
E1
E2
-Vref/2
Vref/2
0.00
Code
50.00

FIG. 11

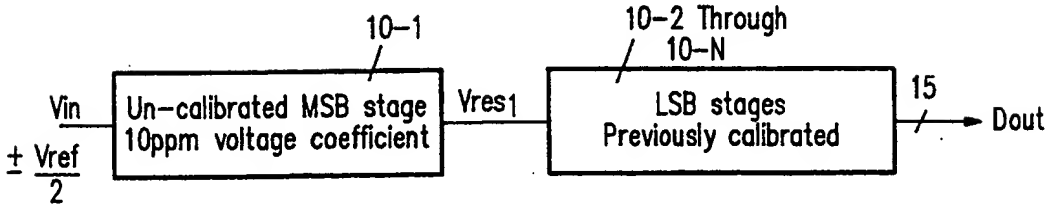

10-1
10-2 Through
10-N
Vin
± Vref/2
Un-calibrated MSB stage
10ppm voltage coefficient
Vres1
LSB stages
Previously calibrated
15
Dout

FIG. 12

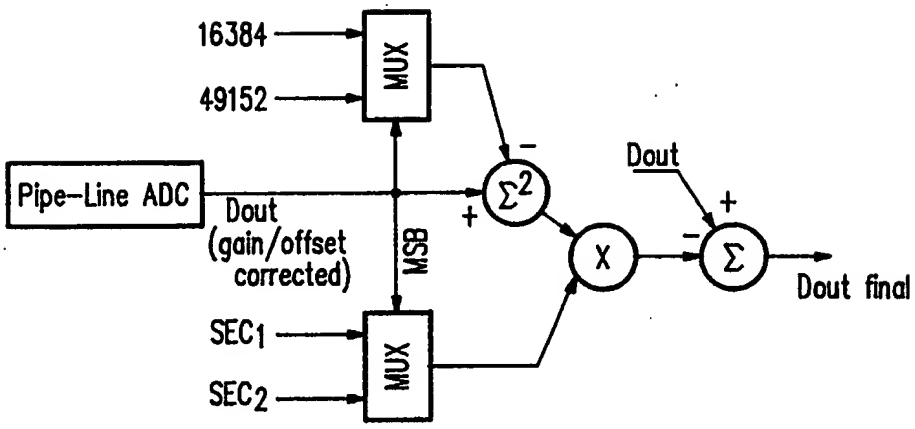

16384
49152
MUX
Pipe-Line ADC
Dout
(gain/offset
corrected)
MSB
SEC1
SEC2
MUX
Σ2
+
−
X
Dout
+
−
Σ
Dout final

FIG. 13

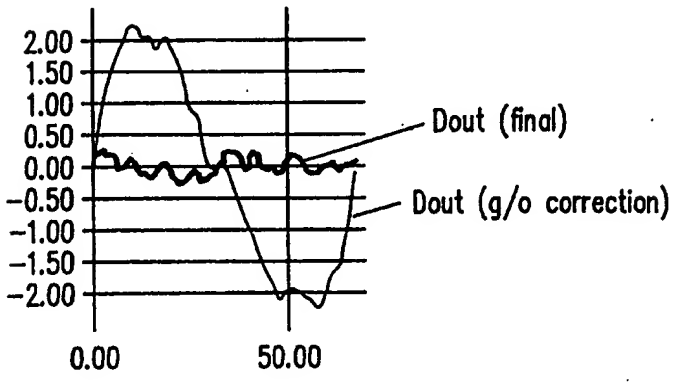

2.00
1.50
1.00
0.50
0.00
−0.50
−1.00
−1.50
−2.00
0.00
50.00
Dout (final)
Dout (g/o correction)

FIG. 14

INTERNATIONAL SEARCH REPORT

Intern. ıal Application No
PCT/US 94/10318

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M1/10 H03M1/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB,A,2 265 775 (HUGHES AIRCRAFT) 6 October 1993	1,4,5,8
A	see page 6, line 20 - page 21, line 19; figure 3	15,19

X	WO,A,89 11757 (HUGHES AIRCRAFT) 30 November 1989	1
A	see page 8, line 13 - page 14, line 28; claim 6; figure 1	2,6-8, 10-13, 15,19

X	US,A,5 047 772 (RIBNER) 10 September 1991	1,8
A	see column 3, line 26 - column 9, line 36; figures 1,4,5	15,19

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 January 1995	17. 01. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Guivol, Y

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INTERNATIONAL SEARCH REPORT

Intern. ..al Application No
PCT/US 94/10318

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 931 797 (KAGAWA ET AL) 5 June 1990 see column 2, line 53 - column 3, line 44 see column 6, line 20 - column 7, line 43; figure 8 -----	1,2,4,8, 15

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern[illegible]nal Application No
PCT/US 94/10318

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		JP-A-	6045938	18-02-94
WO-A-8911757	30-11-89	US-A-	4947168	07-08-90
		DE-D-	68917437	15-09-94
		EP-A-	0373211	20-06-90
		JP-T-	2504459	13-12-90
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		CN-A-	1057136	18-12-91
		EP-A-	0460840	11-12-91
		JP-A-	5083134	02-04-93
		KR-B-	9405935	24-06-94
US-A-4931797	05-06-90	JP-A-	1309419	13-12-89
		JP-A-	1126022	18-05-89